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WHAT IS CLAIMED IS:

1. A data burst transfer circuit comprising:

an oscillation circuit which outputs n (where n is an integer of 2 or above) timing signals of mutually different

5 phases, said oscillation circuit having

a self-oscillation circuit which self-oscillates at a specific frequency;

a frequency divider which outputs the n timing signals based on an output signal of said self-oscillation

10 circuit; and

a control circuit which controls the operation of said self-oscillation circuit and said frequency divider based on a starting signal and a timing signal output from said frequency divider;

15 one or a plurality of parallel-serial conversion circuits which convert n -bit parallel signals into serial signals based on the n timing signals;

one or a plurality of serial-parallel conversion circuits which convert serial signals into n -bit parallel
20 signals based on the n timing signals;

a signal line which transmits serial signals from the parallel-serial conversion circuits to the serial-parallel conversion circuits; and

a signal line which supplies the n timing signals from
25 said oscillation circuit to said parallel-serial conversion

circuits and said serial-parallel conversion circuits respectively.

2. The data burst transfer circuit according to claim
5 1, wherein

said self-oscillation circuit starts self-oscillation when it receives a start signal;

said frequency divider counts the number of oscillation of said self-oscillation circuit and outputs
10 a stop signal when the count reaches the number n; and

said control circuit provides a control to stop the self-oscillation of said self-oscillation circuit when said frequency divider output the stop signal.

15 3. The data burst transfer circuit according to claim 1, wherein said oscillation circuit having,

a self-oscillation circuit which self-oscillates at a frequency which is higher than the frequency of a clock signal;

20 a frequency divider which outputs the n timing signals based on an output signal of said self-oscillation circuit; and

a control circuit which controls the operation of said self-oscillation circuit and said frequency divider based
25 on a starting signal and a timing signal output from said

frequency divider, and

wherein said data burst transfer circuit transfers data at a speed which is higher than the speed of the clock signal.

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4. The data burst transfer circuit according to claim 3, wherein

said self-oscillation circuit starts self-oscillation when it receives a start signal;

10 said frequency divider counts the number of oscillation of said self-oscillation circuit and outputs a stop signal when the count reaches the number n; and

said control circuit provides a control to stop the self-oscillation of said self-oscillation circuit when said
15 frequency divider output the stop signal.

5. The data burst transfer circuit according to claim 1, wherein said parallel-serial conversion circuit converts data read from a memory chip or a memory circuit into serial
20 data, and said serial-parallel conversion circuit outputs data converted into parallel data to a memory chip or a memory circuit.

6. The data burst transfer circuit according to claim
25 5, wherein the starting signal is a pulse signal generated

based on a data read instruction for reading data from said memory chip or said memory circuit.

7. The data burst transfer circuit according to claim
5 5, wherein said oscillation circuit commonly supplies the
n timing signals to said plurality of parallel-serial
conversion circuits that convert one data read from a memory
chip or a memory circuit into serial signals.

10 8. The data burst transfer circuit according to claim
2, wherein said oscillation circuit receives as the starting
signal a signal that is output at a constant timing.

9. The data burst transfer circuit according to claim
15 3, wherein said oscillation circuit receives as the starting
signal a signal that is output at a constant timing.

10. The data burst transfer circuit according to claim
5, wherein said oscillation circuit receives as the starting
20 signal a signal that is output at a constant timing.

11. A parallel-serial conversion circuit comprising:
a self-oscillation circuit which self-oscillates at
a specific frequency, wherein said self-oscillation circuit
25 starts self-oscillation when it receives a start signal;

a frequency divider which outputs n (where n is an integer of 2 or above) timing signals of mutually different phases based on an output signal of said self-oscillation circuit, wherein said frequency divider counts the number
5 of oscillation of said self-oscillation circuit and outputs a stop signal when the count reaches the number n;

a control circuit which controls the operation of said self-oscillation circuit and said frequency divider based on a starting signal and a timing signal output from said
10 frequency divider, wherein said control circuit provides a control to stop the self-oscillation of said self-oscillation circuit when said frequency divider output the stop signal; and

a conversion circuit which convert n-bit parallel
15 signals into serial signals based on the n timing signals.

12. A serial-parallel conversion circuit comprising:

a self-oscillation circuit which self-oscillates at a specified frequency, wherein said self-oscillation
20 circuit starts self-oscillation when it receives a start signal;

a frequency divider which outputs n (where n is an integer of 2 or above) timing signals of mutually different phases based on an output signal of said self-oscillation
25 circuit, wherein said frequency divider counts the number

of oscillation of said self-oscillation circuit and outputs
a stop signal when the count reaches the number n;

a control circuit which controls the operation of said
self-oscillation circuit and said frequency divider based
5 on a starting signal and a timing signal output from said
frequency divider, wherein said control circuit provides
a control to stop the self-oscillation of said
self-oscillation circuit when said frequency divider output
the stop signal; and

10 a conversion circuit which convert serial signals into
n-bit parallel signals based on the n timing signals.

13. An oscillation circuit comprising:

a self-oscillation circuit which self-oscillates at
15 a frequency which is higher than the frequency of a clock
signal;

a frequency divider which outputs n (where n is an
integer of 2 or above) timing signals of mutually different
phases based on an output signal of said self-oscillation
20 circuit; and

a control circuit which controls the operation of said
self-oscillation circuit and said frequency divider based
on a starting signal and a timing signal output from said
frequency divider.

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